IP feedback systems

Alessandro Drago *(INFN - LNF)*

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Luminometry and IP beam monitors for high luminosity
Flavour Factories: techniques and detectors

Introduction

- SuperB needs to align perfectly in horizontal and vertical two ultra-small beams crossing at the IP
- The IP feedbacks can be fundamental systems for assuring stable collisions and luminosity in the SuperB collider
- Different approaches are considered in the following:

  a) "standard" orbit feedback;

  b) luminosity feedback, also called dither feedback, as implemented in PEP-II;

  c) fast IP feedback/feedforward inspired to ILC intrabeam feedback.

Updated parameters table with relevant parameters for feedbacks

Parameter	HER (e^+)	LER (e^-)
Luminosity ($cm^{-2}s^{-1}$)	10^{36}	
E (GeV)	6.7	4.18
C (m)	1205	
Crossing angle (mrad)	60	
Piwinski angle	19.6	17. 5
BB tune shift (x/y)	0.0026/0.11	0.004/0.105
N. bunches	937	
I (mA)	1976	2446
Part/bunch ($x10^{10}$)	5.30	6.56
IP $\beta_{x/y}$ (cm/mm)	2.6/0.253	3.2/0.205
$\varepsilon_{x/y}$ (nm/pm) (with IBS)	2.26/5.7	2.29/5.7
IP $\sigma_{x/y}$ (mm/nm)	7.7/38	8.6/34
σ_l (mm)	5	5
Polarization (%)		80

Collision with so small beams can be not a trivial task!

- Comparing DAFNE and SuperB beam transverse parameters:
  - DAFNE sigmaX@SLM = 1-1.2 mm
  - DAFNE sigmaY@SLM = 200-260 micron
  - DAFNE stay clear > 2 cm

  - SuperB sigmaX@IP = 7.7 – 8.6 micron
  - SuperB sigmaY@IP = 38 – 34 nm
  - SuperB stay clear = 30 sigma ~= 270 micron?

What Dynamic Range do we need ? As well known D.R. is the ratio between the largest and smallest possible values of a signal. It is measured as a ratio, or as a base-10 (deciBel) logarithmic value.

- DAFNE horizontal minimum dynamic range:
  20*log10(2cm/1mm)=20*log10(2000)=20*3.3=**66dB**
- DAFNE vertical minimum dynamic range:
  20*log10(2cm/0.2mm)=20*log10(10000)=20*4=**80dB**
- Considering the analog to digital converter (ADC) dynamic range:

  20*log10((2**Nbit)/1)= (Nbit*6.02) dB

  - 8 bit ADC = 48 dB
  - 10 bit ADC = 60 dB
  - 12 bit ADC = 72 dB
  - 14 bit ADC = **84 dB** **** it should be enough!!
  - 16 bit ADC = 96 dB
- For SuperB: 20*log10(30sigma/sigma)=20*1.5=**30dB** (<u>it seems too low!</u>)

Orbit feedback

(often called FOFB, Fast Orbit FeedBack)

The logic that driver this system is to have a data processing unit for each BPM, to build a beam orbit fro each ring in real time (1-10kHz), to compare it with a golden orbit and to apply a new set to the best corrector.

PERFORMANCE AND FUTURE DEVELOPMENT OF THE DIAMOND FAST ORBIT FEEDBACK SYSTEM

M. G. Abbott, J. A. Dobbing, M. T. Heron, G. Rehm, J. Rowland, I. S. Uzun, Diamond Light Source, Oxfordshire, U.K. S. Duncan, University of Oxford, Oxfordshire, U.K

INTRODUCTION

The Fast Orbit Feedback (FOFB) system on the Diamond Light Source storage ring began routine operation in July 2007. It achieves integrated beam stability, up to 100 Hz, of X < 1.0 μm and Y < 0.4 μm, at primary eBPMs, which are well within the required 10% RMS beam dimensions. The FOFB implementation has been refined during this operational period to improve stability and to cope with anomalous behaviour in eBPMs and the communications network.

While the FOFB meets the current requirements it is recognised that the system needs to be further developed to meet increasing demands on beam stability, arising from smaller vertical beam sizes, higher sensitivity beamlines and additional sources of beam motion.

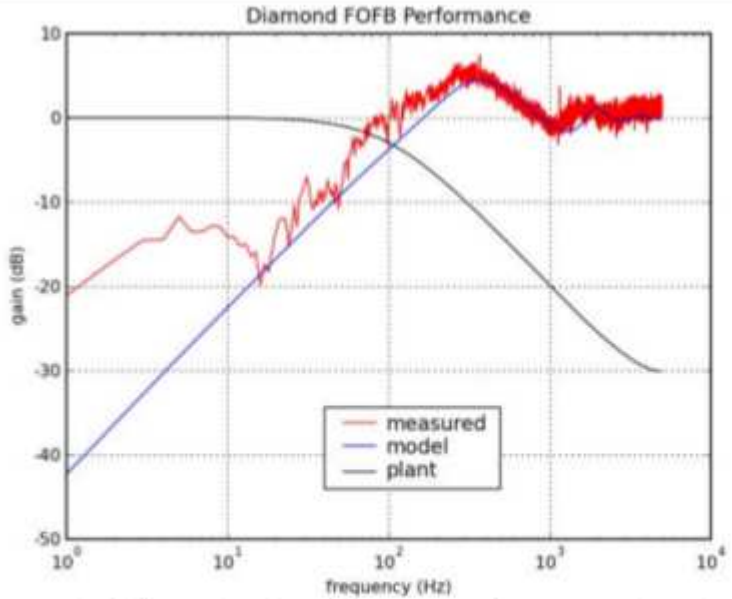


Figure 3: Theoretical and measured suppression in the vertical plane. Below 10 Hz is noise dominated in the measured data.

A real case from Diamond Light Source (Univ.of Oxford), one ring

2012 data sheet

Benefits

Libera Brilliance+ enable beam signal processing and fast global orbit feedback building.

Latest technology embedded

- VirtexTM 5
- 16-bit ADC
- GbE ready
- COM Express Basic module with Intel Atom N270 (x86), upgradable

Basic Application Support Environment

Performance specification

- Turn-by-turn resolution: < 0.5 um typical value (0 dBm, ~ 300 kHz revolution frequency)
- Slow monitoring resolution: ~10 nm typical value(0 dBm, 10 Hz data rate)
- Beam current dependence: 1 um (0 dBm --> -50 dBm)

Feature highlights

- Time Domain Processing for precise measurements with single bunch / short fill pattern
- Deep memory buffer for raw ADC data (8 ms)

Orbit feedback based on “intelligent” data acquisition system

a) The choice could be similar to the same system used in DIAMOND and in other accelerators (Libera by I-Tech ?)

b) Implemented in many circular light sources but still not (?) in a circular collider that means two rings with a common IP area

c) The input signal should have ~2kHz bandwidth (considering 10kHz of sampling rate)

d) How fast can corrector magnet be set? 10Hz? 100Hz? More?

e) ~1 micron overall stability/sensitivity (?)

f) Strategy: in each ring the feedback operates to move orbit toward the reference orbit applying command to the “regular” correctors

g) At the IP (that is a common part of the vacuum chamber) it is necessary to avoid unstable situations or conflicts between the two orbit feedback systems

Luminosity feedback
(or dither feedback)

This system is implemented by dither coils in the IP region and receives fast data from luminometer system

A PROPOSED FAST LUMINOSITY FEEDBACK FOR THE SUPER-B ACCELERATOR*

Kirk Bertsche#, R. Clive Field, Alan Fisher, Michael Sullivan, SLAC, Menlo Park, CA 94025, USA
Alessandro Drago, INFN/LNF, Frascati (Roma), Italy

Abstract

We present a possible design for a fast luminosity feedback for the SuperB Interaction Point (IP). The design is an extension of the fast luminosity feedback installed on the PEP-II accelerator. During the last two runs of PEP-II and BaBar (2007-2008), we had an improved luminosity feedback system that was able to maintain peak luminosity with faster correction speed than the previous system. The new system utilized fast dither coils on the High-Energy Beam (HEB) to

For SuperB, we have the advantage of including a fast feedback system in the original design rather than trying to retrofit one later. We propose a similar system to PEP-II, but with dithering of the Low-Energy Beam (LEB) rather than the HEB and use of a higher frequency (1-3 kHz). Simultaneous excitation with lock-in amplifiers should allow corrections to about 300 Hz. We will also investigate sequential excitation, which may allow faster corrections of the more critical y position. The best feedback approach will be dependent on the noise environment, which will not be known until the machine is commissioned, so the system must be flexible.

DITHER COILS

Coil Locations

nagnets (see Fig. 1).

SuperB

Fast Luminosity Feedback

Super-B
2-13-09

Kirk Bertsche

PEP-II poster presented at EPAC'06 and PAC'07. The upgraded version at the VIII SuperB General Meeting and at PAC'09 by **Kirk Bertsche**

IP “Dither” (Luminosity) feedback

I. The old IP “Dither” feedback system was designed in 2006 for PEP-II using dedicated corrector magnets and luminosity signal to optimize the overlap of colliding beams at the interaction point.

II. The luminosity signal comes from a real time luminosity detector (with very fast response, but not necessarly bunch-by-bunch because the bandwidth is 500 Hz).

III. One beam (HEB , high-energy beam) is steered through the IP to maximize the signal from the detector.

IV. The other beam (LEB), is driven with small dither motions 1 to 3 kHz to allow luminosity detection of best beam overlap.

V. The dither and applied corrections occur in three directions: horizontal, vertical, and vertical angle.

VI. The SuperB design allows for dither amplitudes of up to 25 microns horizontal, 2 microns vertical, and >0.5 mrad in vertical angle.

VII. Relative to the IP, the dither coils inSuperB are foreseen at ±3.5 meters and ±15 meters, with horizontal and vertical pairs at each location.

Luminosity Feedback

- PEP-II dithered LER position and angle against HER
  - Initially dithered x, y, and y' sequentially, in steps
  - Later simultaneously, with small sinusoidal drive at 3 frequencies
  - Rate limited to 1 Hz by software magnet controls
  - Often ran at 0.3 Hz to use smaller dithers
- Integrate luminosity feedback with orbit feedback !!!
  - Avoids having orbit feedback "fix" the luminosity dither
    - Especially in x, which the BPMs will see

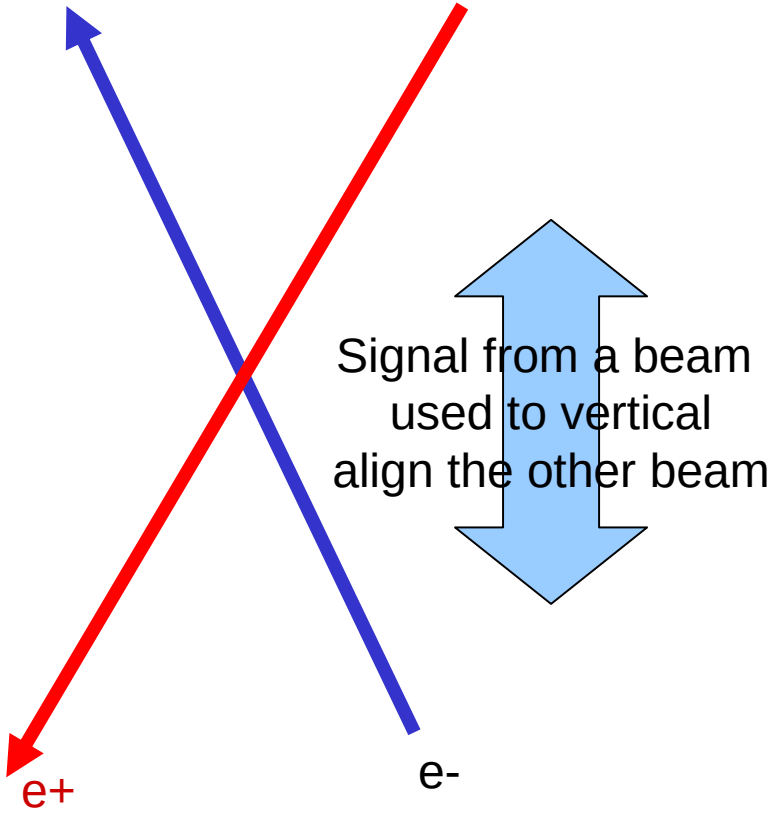
Important comment by Alan Fisher

Fast IP feedback

Faster than the previous systems, this feedback reads position from both beams, comparing them and kicking one beam to adjust trajectory

Fast IP feedback (or feedforward)

- This design is freely inspired to the FONT project (by P. Burrows, John Adams Inst., Oxford)
- Design is in preliminary phase
- STRATEGY: The feedback should take the vertical position of the first and second beam moving vertically the second beam for a better very fast overlap in the Interaction Point



Fast Feedback development at ATF, and relevance to SuperB

Glenn Christian, Phil Burrows, Colin Perry
John Adams Institute, University of Oxford

SuperB mini-workshop, Oxford,
18 May 2011

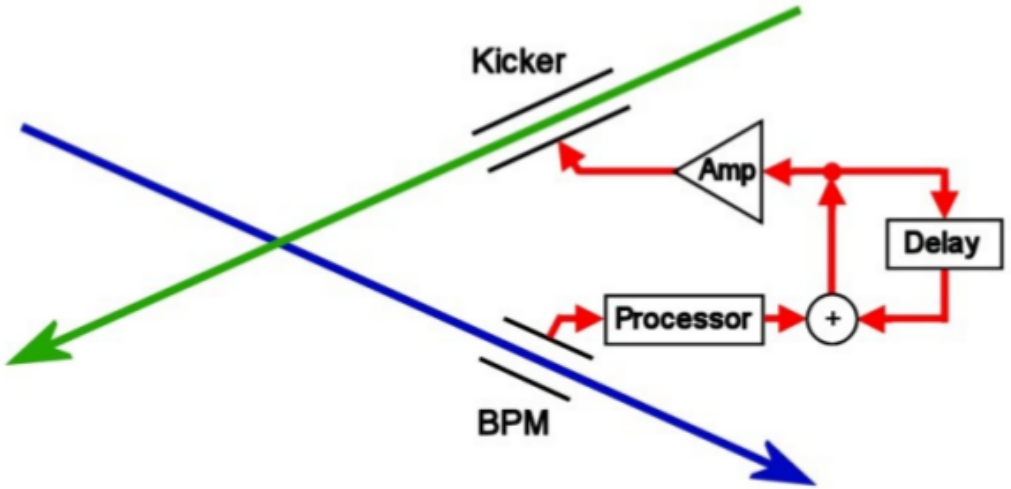
SuperB FB requirements

(from discussion with Marica Biagini and Alessandro Drago)

- Spot size at IP: 36 nm (y) by 7-9 um (x)
- Stability: 10 nm @ IP
- As well as orbit correction feedback, requirement for IP feedback to correct for ground motion, vibrations – cause beam jitter and lumi loss

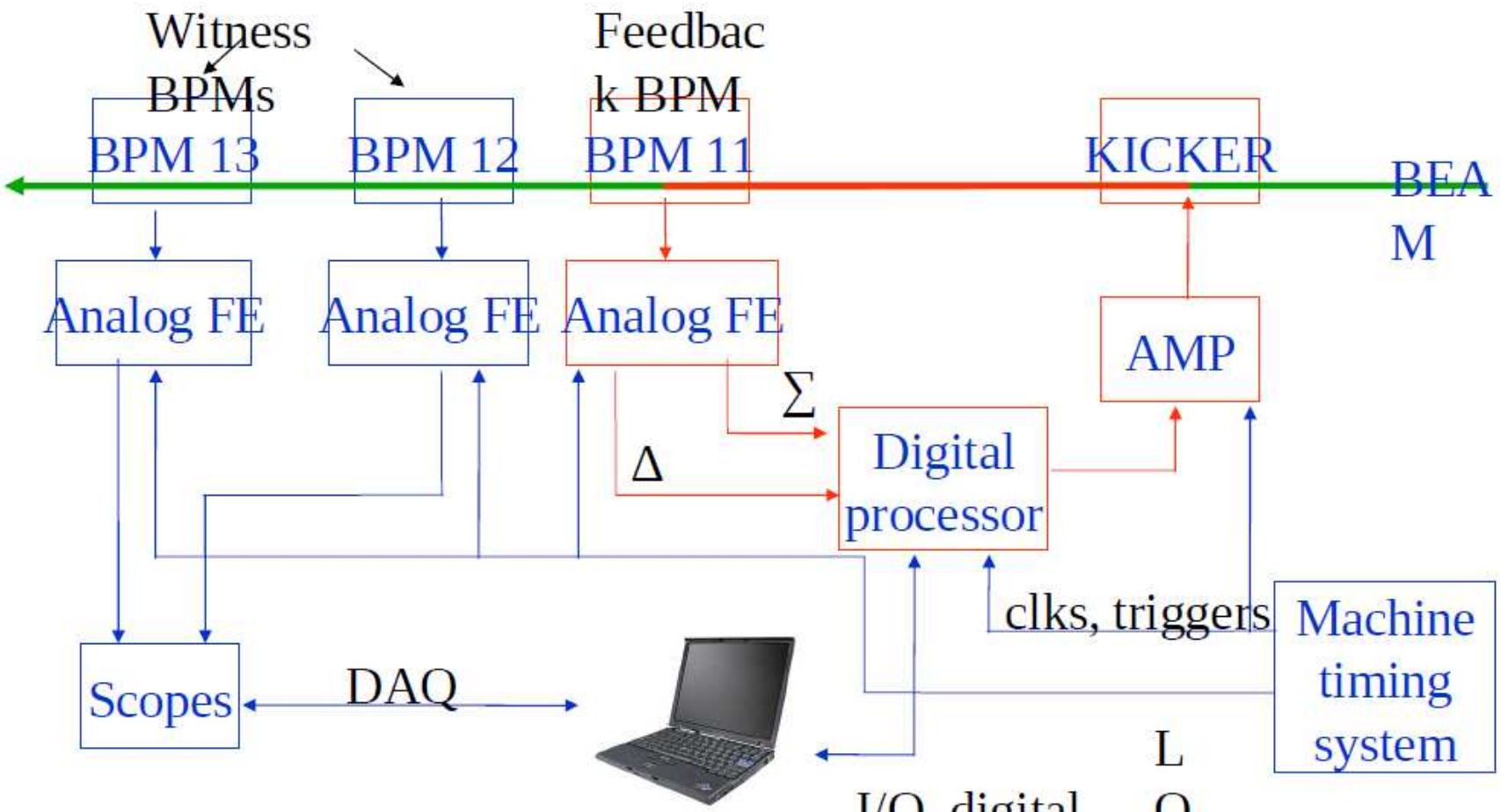
ILC IP Feedback system - concept

- Several slower beam-based feedbacks/feedforwards required for orbit correction
- Fast intra-train feedback system essential for the ILC interaction point to compensate for relative beam misalignment.
- Measure vertical position of outgoing beam and hence beam-beam kick angle
- Use fast amplifier and kicker to correct vertical position of beam incoming to IR
- Delay loop necessary to maintain the correction for subsequent bunches in the train

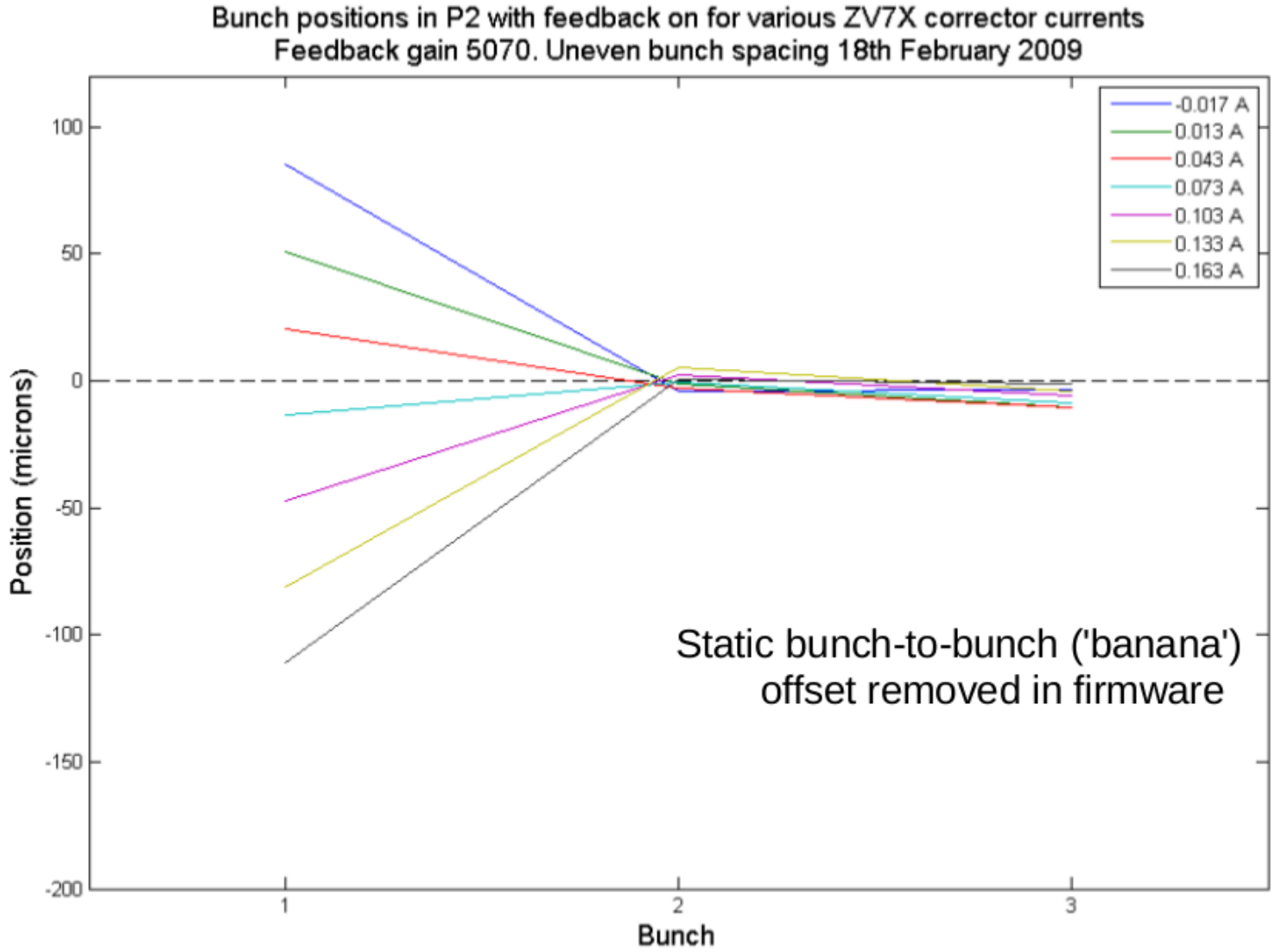


Last line of defence against relative beam misalignment

FONT4 system overview



Feedback Performance (1) – Offset correction/gain optimisation (averaged over ~50 pulses per point)



FB Considerations

- BPM processor
  - Main question is measurement location and hence required BPM resolution
  - Bunch-by-bunch measurement (i.e. do we need to resolve individual bunches) or integrating continuous beam ?
    - Current processor output has width of ~10 ns, can be tweaked by changing the filtering(possibly at the cost of resolution)
    - If mixing with 714 MHz, then integrating will not work at 2.1 ns bunch spacing.
  - Processor type: mixer or baseband (better resolution, better suited to bunch-by-bunch measurement)
  - If new processors required, what is the availability of test beams?
- Feedback
  - Averaging (slower) or minimum latency (fastest, but may introduce extra noise) – needs detailed optimisation
- Amplifier
  - Would require continuous rated amplifier rather than pulsed – less kick for the same power
  - Power: tradeoff of dynamic range and resolution ?
  - Multiple kickers, if larger dynamic range needed?
- Next step:
  - Study the lattice and define optimal location for BPM and kicker
  - Determine required resolution, dynamic range, and required amplifier power

Fast IP feedback

- Why another feedback ?
- Many reasons:
  - The betatron and synchrotron bunch-by-bunch feedback work as band pass filter and cannot do almost anything about slow motions
  - Luminosity and orbit feedbacks will realistically work between 100Hz and 1kHz
  - There are mid-frequency motion range to be considered (1kHz-1MHz)
  - Each corrector magnet transitions can produce losses of luminosity if not perfectly synchronized (for bad overlapping)
  - The Fast IP feedback must make a beam able to overlap the other beam as a vertical follower for the necessary short period of time
  - What about horizontal and angle ? Also these options in principle could be considered

Fast IP feedback or feedforward ("beam-follower")

Tentative specifications and algorithm

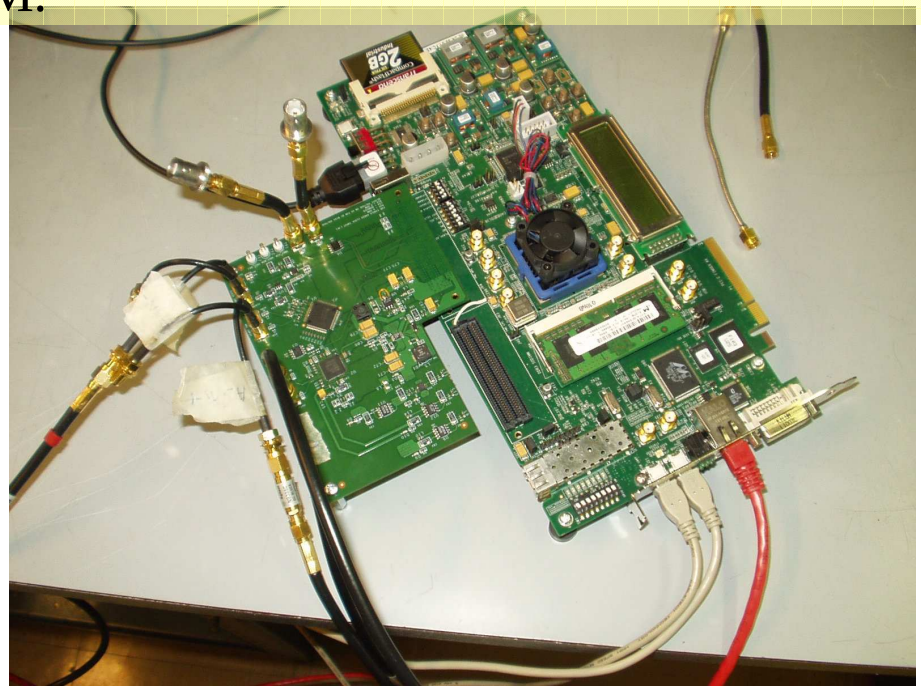
- Propagation delay: ~150ns
- It should be able to acquire position signals with a precision better than 36 nm from the first and the second beam
- It should be compute average values from 30-40 bunch trains for e+ and e- beams
- It should compare the two signals (avoiding noise problems) and generate a correction signal to be applied to the second beam that have to be perfectly overlapped to the first beam
- Bandwidth: at least up to revolution frequency, better if up to 1MHz
- Great noise immunity is fundamental
- Dynamic range: the feedback should work at least between 10 nm and ± 10 μm, so the minimum is 60dB, better if >70dB
- It should be based on FPGA to be extremely flexible and to give possibility to try different feedback transfer functions & algorithms
- Powerful software to monitor and change parameters in real time

Fast IP feedback (or feedforward)

Parts under study that could be used for implementation:

- ML605 by Xilinx with the last Virtex-6 FPGA
- ADS 5474 (Analog-to-digital converter) by Texas Instruments:
  * 400-MSPS Sample Rate
  * 14-Bit Resolution, 11.2-Bits ENOB
  * 1.4-GHz Input Bandwidth
  * SFDR = 80 dBc at 230 MHz and 400 MSPS
  * SNR = 69.8 dBFS at 230 MHz and 400 MSPS
  * 2.2-Vpp Differential Input Voltage
  * LVDS-Compatible Outputs
- MAX 5891 by Maxim: 16-Bit, 600Msps, High-Dynamic-Performance DAC with LVDS Inputs

From digital acquisition point of view, this FPGA-based ML605 board by Xilinx has been tested. It has a custom 14-bit ADC/DAC mezzanine board with FMC interface. The system has been used in May 2012 to acquire DAFNE e+ beam data from a BPM.



Low-cost pc motherboard that can accept 7 PCI-express boards on the bus and can be used as main processing unit

TIMING MODULE

a multiple channel data acquisition system that works in parallel needs an efficient clock and trigger management. A custom module with functionality of distributing and timing the 7 DAS has to be designed & built. The goal is to be able to de-skew individually the sampling frequency for each channels and also to interface the start acquisition trigger. If programmed adequately, this module can also make the data acquisition for both longitudinal and transverse signal detection.

This low cost digital delay lines will be the base of the timing module

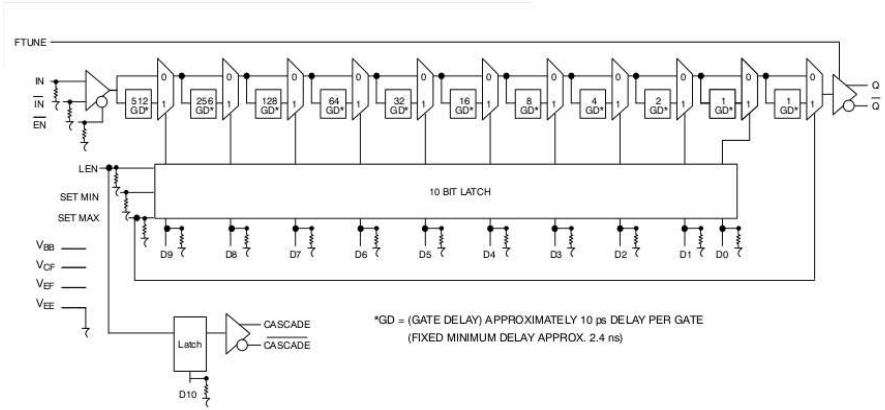
Range 0-10ns

Step 10 ps

Max clock frequency 1.2GHz

It works as negative or positive ECL

Data lines D[10:0] can accept ECL, LVCMOS and LVTTL



MC100EP196

MC100EP196

3.3V ECL Programmable Delay Chip with FTUNE

The MC100EP196 is a programmable delay chip (PDC) designed primarily for clock deskewing and timing adjustment. It provides variable delay of a differential NECL/PECL input transition. It has similar architecture to the EP195 with the added feature of further tuneability in delay using the FTUNE pin. The FTUNE input takes an analog voltage from V_{CC} to V_{EE} to fine tune the output delay from 0 to 60 ps.

The delay section consists of a programmable matrix of gates and multiplexers as shown in the logic diagram, Figure 2. The delay increment of the EP196 has a digitally selectable resolution of about 10 ps and a net range of up to 10.2 ns. The required delay is selected by the 10 data select inputs D[9:0] values and controlled by the LEN (pin 10). A LOW level on LEN allows a transparent LOAD mode of real time delay values by D[9:0]. A LOW to HIGH transition on LEN will LOCK and HOLD current values present against any subsequent changes in D[10:0]. The approximate delay values for varying tap numbers correlating to D0 (LSB) through D9 (MSB) are shown in Table 5.

Because the EP196 is designed using a chain of multiplexers, it has a fixed minimum delay of 2.4 ns. An additional pin, D10, is provided for controlling Pins 14 and 15, CASCADE and $\overline{\text{CASCADE}}$, also latched by LEN, in cascading multiple PDCs for increased programmable range. The cascade logic allows full control of multiple PDCs. Switching devices from all "1" states on D[0:9] with SETMAX LOW to all "0" states on D[0:9] with SETMAX HIGH will increase the delay equivalent to "D0", the minimum increment.

Select input pins, D[10:0], may be threshold controlled by combinations of interconnects between V_{EF} (pin 7) and V_{CF} (pin 8) for LVCMOS, ECL, or LVTTL level signals. LVTTL and LVCMOS operation is available in PECL mode only. For LVCMOS input levels, leave V_{CF} and V_{EF} open. For ECL operation, short V_{CF} and V_{EF} (pins 7 and 8). For LVTTL level operation, connect a 1.5 V supply reference to V_{CF} and leave open V_{EF} pin. The 1.5 V reference voltage to V_{CF} pin can be accomplished by placing a 2.2 kΩ resistor between V_{CF} and V_{EE} for 3.3 V power supply.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single−ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

The 100 Series contains temperature compensation.

- Maximum Frequency > 1.2 GHz Typical
- Programmable Range: 0 ns to 10 ns
- Delay Range: 2.4 ns to 12.4 ns
- 10 ps Increments
- PECL Mode Operating Range: V_{CC} = 3.0 V to 3.6 V with V_{EE} = 0 V
- NECL Mode Operating Range: V_{CC} = 0 V with V_{EE} = −3.0 V to −3.6 V
- Open Input Default State
- Safety Clamp on Inputs
- A Logic High on the $\overline{\text{EN}}$ Pin Will Force Q to Logic Low
- D[10:0] Can Accept Either ECL, LVCMOS, or LVTTL Inputs
- V_{BB} Output Reference Voltage
- Pb−Free Packages are Available*

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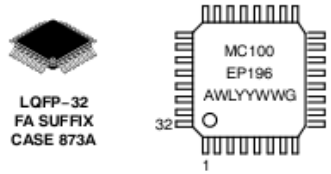
http://onsemi.com

MARKING DIAGRAM*



LQFP−32
FA SUFFIX
CASE 873A

A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

*For additional marking information, refer to Application Note AND8002/D.

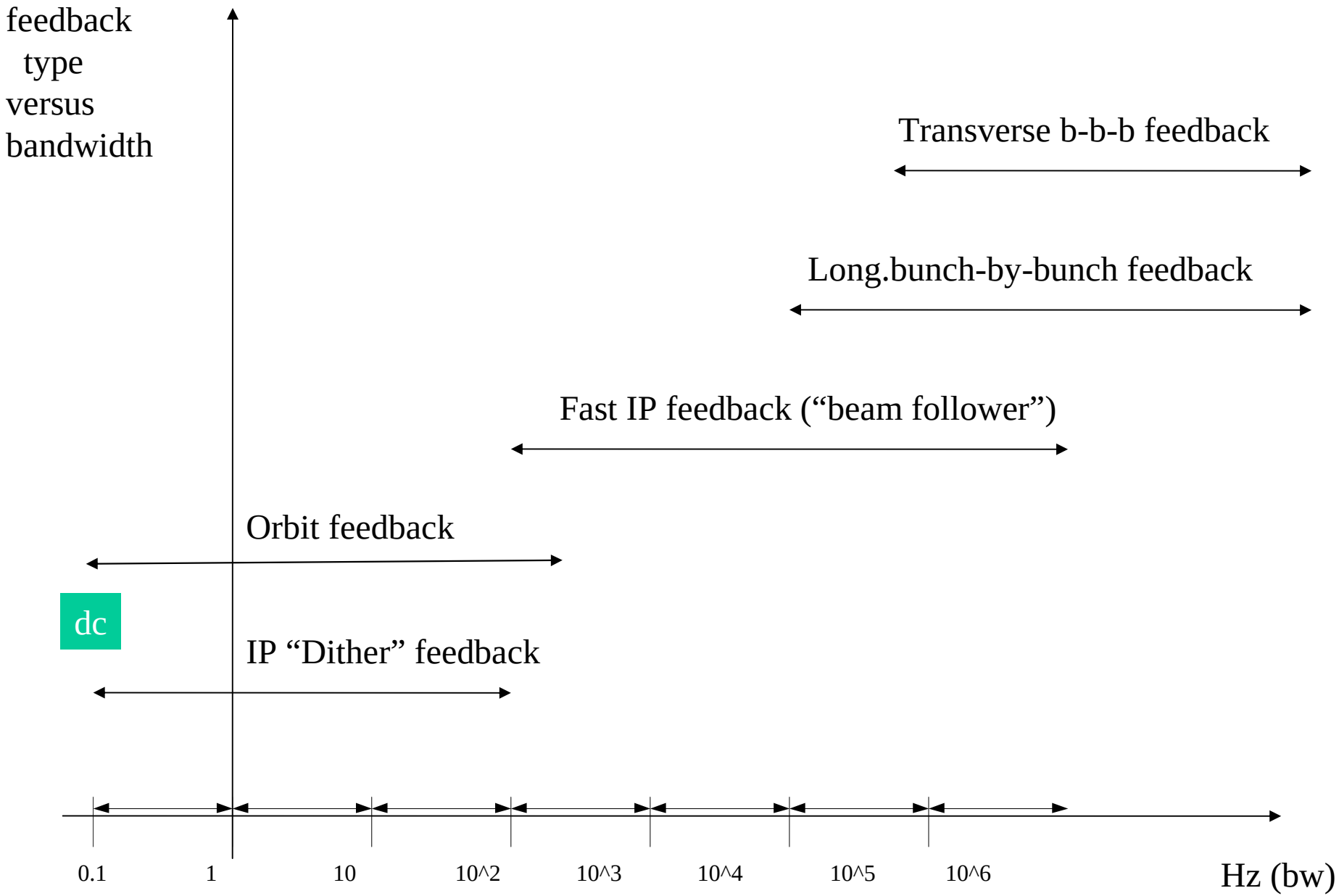
ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 17 of this data sheet.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

As summary: multiple feedback systems to maintain stable collisions

- *Synchrotron bunch-by-bunch feedback systems*: these are used to maintain under control the longitudinal bunch-by-bunch motions (kicking each bunch every turn in the longitudinal planes)
- *Betatron bunch-by-bunch feedback systems*: these are used to maintain under control the transverse bunch-by-bunch motions (kicking each bunch every turn in vertical & horizontal planes)
- *Orbit feedback* (Libera or Libera–like based): it takes as reference a “golden orbit” for each ring and applies corrections using the “regular” corrector magnets
- *IP “dither” feedback (or luminosity feedback)*: it should use 4 (dual-axis) air-core coil correctors to generate orbit-bumps in 3 dimension (in just one of the two rings) being based on the Luminosity monitor real-time data
- *Fast IP feedback* (“beam-follower”): this system, freely inspired to FONT project, is in R&D phase.


feedback
type
versus
bandwidth
Transverse b-b-b feedback
Long.bunch-by-bunch feedback
Fast IP feedback (“beam follower”)
Orbit feedback
dc
IP “Dither” feedback
0.1
1
10
10^2
10^3
10^4
10^5
10^6
Hz (bw)

Conclusions

To achieve the Superb luminosity specifications a perfect bunch-by-bunch overlap of the two beams is necessary.

- Diagnostic and feedback systems are crucial to achieve the luminosity goal
- Three different feedback systems have been considered
- The systems should and can have cooperating behavior
- Orbit feedback and luminosity feedback should be implemented taking in mind the previous design experiences
- Luminosity (dither) feedback needs a special interface to a fast luminometer
- R&D on Fast IP feedback is in progress